High Speed FPGA-Based Radiation Signal Emulator

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Abstract— **Reliable verification of nuclear instrumentation and control(I&C) requires a realistic reactor environment, but direct testing on plant hardware is constrained by radiation safety and outage risk. This work presents an FPGA-based real-time signal emulator that generates radiation-origin signals on a single platform. Implemented on a Xilinx KCU105 running at 250 MHz, the prototype showed clearly separable neutron and gamma components at 20 dB SNR and 10^0% reactor power and achieved speedups of 15× over MATLAB, 7× over Python, and 5× over C for a one-minute scenario. These results demonstrate fast, repeatable, and safe I&C verification without a reactor, supporting real-time or near-real-time testing.**

Keywords; FPGA; Signal Emulator; Nuclear Engneering;

I. INTRODUCTION

Reliable verification of the functionality and performance of nuclear power plant instrumentation and control(I&C) systems requires realistic test stimuli that emulate physical phenomena across the full operating range. However, direct interfacing with actual plant equipment is inappropriate due to radiation safety and potential shutdown constraints, necessitating a signal generator and emulator capable of providing equivalent stimuli without the plant. Purely software-based simulation of radiation-origin signals and electrical noise at high resolution over long durations becomes computationally prohibitive and thus impractical. To overcome these limitations, this paper proposes an FPGA-based real-time signal emulator that synthesizes radiation-origin output signals on a single platform and, by exploiting hardware parallelism, enables fast, repeatable, and safe verification of instrumentation and control systems without a reactor.

II. PROPOSED METHOD

Radiation produced by fission inside a reactor, principally neutrons, gamma rays, and, alpha particles, is detected by the fission chamber[1, 2]. In particular, the primary inputs to the I&C systems, the neutron n and gamma ray γ signals, can be modeled as tail pulse electrical waveforms, as in (1). The shape of an individual pulse is governed by three
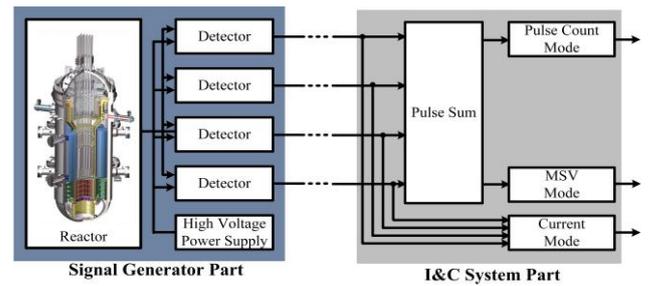
Figure. 1. Block diagram of the signal generator and the I&C system.

parameters: rise time constant T_r, fall time T_f, and peak amplitude scaling factor I_{max}[3].

$$i_n(t) = I_{n,max} \times (e^{-t/T_{n,f}} - e^{-t/T_{n,r}}),$$
$$i_\gamma(t) = I_{\gamma,max} \times \left(e^{-t/T_{\gamma,f}} - e^{-t/T_{\gamma,r}}\right) \quad (1)$$

The noise signal is modeled as AWGN and, based on the SNR, is represented as shown in (2).

$$P_{noise} = P_{signal} \times 10^{-(SNR/10)}$$
$$\xi(t) \sim \mathcal{N}(0, P^2_{noise}) \quad (2)$$

Because neutron and gamma-ray emission times are typically approximated by a stochastic process, the waveform observed by the I&C systems appears as a temporally overlapping train of pulses. The overall signal therefore consists of neutron, gamma-ray, and electrical noise components, and is expressed as in (3).

$$i_q(t) = \sum_{i=1}^{K} \{i_n(t - t_{n,i}) + i_\gamma(t - t_{\gamma,i})\} + \xi(t) \quad (3)$$

Let K be the pulse count, proportional to reactor power. With neutron and gamma-ray signals measured in electrical noise, higher power increases K, deepens pulse overlap, and propor-
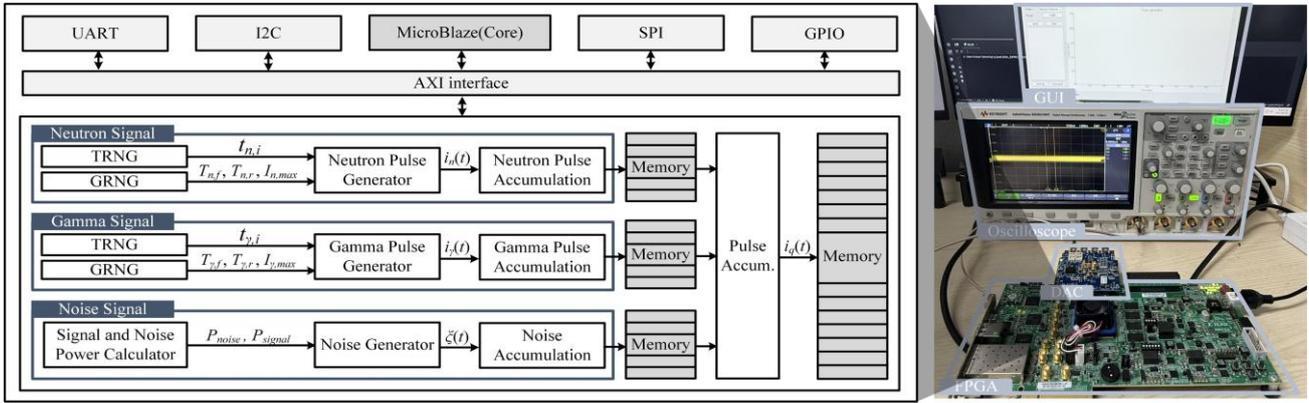
Figure. 2.   FPGA architecture of the proposed signal emulator

-tionally raises the composite signal level. Fig. 2 depicts the overall architecture of the proposed signal emulator. When the reactor power, signal to noise ratio, and simulation time are set in the host GUI, the parameters are sent to the FPGA via UART, and the FPGA synthesizes the signals accordingly. First, the neutron pulse occurrence times $t_{n,i}$ are generated by true random number generator (TRNG) implemented with a linear feedback shift register LFSR. $T_{n,r}$, $T_{n,f}$, and $I_{n,max}$ are drawn from a Gaussian random number generator (GRNG) using the Box Muller method. The neutron pulse generator block synthesizes the waveform in accordance with (1) using these parameters, and the resulting sequence is accumulated in dedicated memory. The gamma signal is generated in the same manner as the neutron signal. The noise component is produced by first computing the P_{noise} from the reference P_{signal} and the target SNR, then generating the sequence according to (2) in the noise generator and storing it in memory. Neutron, gamma, and noise signals are generated simultaneously in parallel. Finally, the three components are summed on the time axis to form the output sequence $i_q(t)$ The resulting waveform is streamed to the host via UART for real-time visualization and logging in the GUI, and it is also output as an analog signal through the DAC.

III.   EXPERIMENTAL RESULTS AND CONCLUSION

The proposed signal emulator was implemented on the Kintex UltraScale FPGA of a Xilinx KCU105 board and operates at 250 MHz. Fig. 3 presents time-domain waveforms synthesized at 20 dB SNR with a single gamma and a single neutron component; their different peak locations make them clearly separable and stably identifiable. Fig. 4 compares execution times for software on an Intel Core i7-12700 (MATLAB R2024b, Python in PyCharm 2024.2.4, and C with MS Visual Studio 2022) and the FPGA design using a one-minute simulation at 20 dB SNR. The FPGA ran about fifteen times faster than MATLAB, seven times faster than Python, and five times faster than C, demonstrating suitability for real- or near-real-time generation. in conclusion, the hardware-accelerated emulator enables fast, repeatable, and safe I&C verification without a reactor and scales via its modular design to multi-channel operation and diverse detector characteristics.
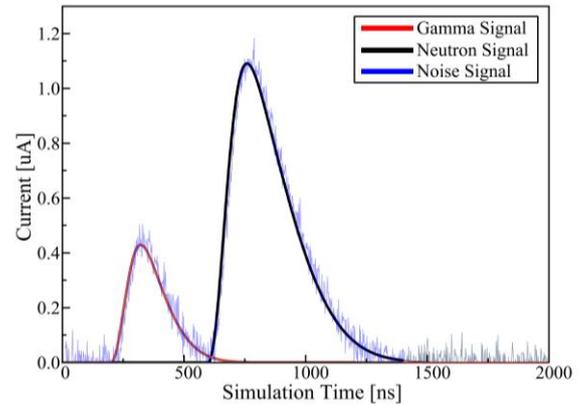

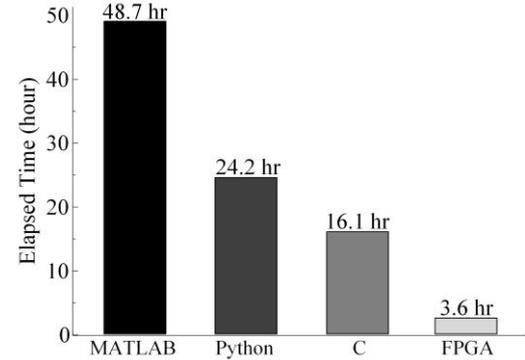Figure. 3.   Output waveforms at neutron, gamma, and noise signals

Figure. 4.   Elapsed time MATLAB, Python, C, and FPGA at power 10^0%

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